What is claimed is:

1. A method for depositing multiple metal layers on a semiconductor substrate, comprising:

contacting a semiconductor substrate with an electrolytic plating composition, the plating composition comprising a copper metal source and a second metal source distinct from copper;

electrolytically depositing a first metal layer of copper on the semiconductor substrate at a first reduction potential;

electrolytically depositing a second metal layer on the semiconductor substrate at a second reduction potential distinct from the first reduction potential.

2. The method of claim 1 wherein the first metal layer is a substantially homogenous copper metal layer.

3. The method of claim 1 wherein the second metal layer is a copper alloy.

4. The method of claim 1 wherein the second metal layer comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver, and cadmium.

5. The method of claim 1 wherein the second metal layer is a copper alloy that comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver, and cadmium.

6. The method of claim 1 wherein the first and second reduction potentials differ by at least about 0.2 V.

7. The method of claim 1 wherein a plurality of first metal layer are deposited with a plurality of alternating second metal layers.

8. The method of claim 1 wherein the first metal layer is effectively conductive and the second metal layer is substantially less conductive than the first layer.

9. The method of claim 1 wherein the first metal layer functions as an electrical circuit, and the second metal layer functions as an insulator layer.

10. The method of claim 1 wherein the substrate is a lead of a semiconductor device, or an interconnect of a semiconductor device.

11. A method for depositing multiple metal layers on a printed circuit board substrate having circuitry thereon, comprising:

contacting a printed circuit board substrate with an electrolytic plating composition, the plating composition comprising a copper metal source and a second metal source distinct from copper;

electrolytically depositing a first metal layer of copper on the printed circuit board substrate at a first reduction potential;

electrolytically depositing a second metal layer on the printed circuit board substrate at a second reduction potential distinct from the first reduction potential.

12. The method of claim 11 wherein the first metal layer is a substantially homogenous copper metal layer.

13. The method of claim 11 wherein the second metal layer is a copper alloy.

14. The method of claim 11 wherein the second metal layer comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver, and cadmium.

15. The method of claim 11 wherein the second metal layer is a copper alloy that comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver, and cadmium.

16. The method of claim 11 wherein the first and second reduction potentials differ by at least about 0.2 V.

17. The method of claim 11 wherein a plurality of first metal layer are deposited with a plurality of alternating second metal layers.

18. The method of claim 11 wherein the first metal layer is effectively conductive and the second metal layer is substantially less conductive than the first layer.

19. The method of claim 11 wherein the first metal layer functions as an electrical circuit, and the second metal layer functions as an insulator layer.

20. The method of claim 11 wherein a solder material is deposited on the substrate.

21. A method for depositing multiple metal layers on an electronic device substrate, comprising:

contacting the electronic device substrate with an electrolytic plating composition, the plating composition comprising a first metal source and a second metal source distinct from the first metal;

electrolytically depositing a layer of the first metal layer on the substrate at a first reduction potential;

electrolytically depositing a second metal layer on the substrate at a second reduction potential distinct from the first reduction potential.

22. The method of claim 21 wherein the substrate is a semiconductor substrate.

23. The method of claim 21 wherein the substrate is a semiconductor package substrate.

24. The method of claim 21 wherein the substrate is a multi-chip module, chip capicator, chip resistor, lead frame, or an opto-electronic device.

25. The method of claim 21 wherein the first metal layer is a substantially homogenous tin metal layer.

26. The method of claim 21 wherein the second metal layer is a tin alloy.

27. The method of claim 21 wherein the second metal layer comprises one or more of zinc, nickel, silver,antimony, bismuth, indium, cobalt, and copper.

28. The method of claim 21 wherein the first and second reduction potentials differ by at least about 0.2 V.

29. The method of claim 21 wherein a plurality of first metal layer are deposited with a plurality of alternating second metal layers.

30. The method of any one of claims 21 through 30 wherein the first metal layer is effectively conductive and the second metal layer is substantially less conductive than the first layer.

31. The method of claim 21 wherein the first and second metal layers are deposited from a single plating bath.